Remarks

In the Office action, claims 1-8 were rejected under 35 USC § 102 as being anticipated by U.S. Patent No. 5,108,939 to Manley et al. As the Examiner has correctly described, the Manley et al. patent teaches a method and structure of forming a non-volatile memory device that share some features with the present invention. For instance, they both have a thin polysilicon structure in the form of a quarter-sawn ellipse that serves as part of a floating gate structure that extends into the tunneling region of the floating gate. However, there are also major differences that distinguish the present invention from the Manley et al. patent.

One of the most important differences concerns the way the floating gate extension is connected to the floating gate. In all embodiments described in the Manley et al. patent, the floating gate extension is connected only to the sidewall of the floating gate, which has been covered with a thin layer of thermally grown oxide (409 in Figure 4D and 509 in Figures 5E and F). To complete the electrical connection from the floating gate extension to the floating gate, the Manley et al. patent teaches (in col. 5, lines 14-21 and Figure 4E) the use of a photoresist mask 412 to form openings that allow electrical contact between the floating gate extension and the floating gate.

In contrast, the present invention teaches the use of a layer of polysilicon (251 in Figure 2G) as a bridge to connect the floating gate extension 239 to the floating gate 212 through an opening 248 at the top of the floating gate 212. The claims, as amended, clearly distinguish this particular feature of the present invention. As it is stated in claim 1, "a floating gate region and a small sidewall spacer electrically coupled together by a connecting layer, said connecting layer being formed OVER and in contact with both said small sidewall spacer and said main floating gate region." Such construction allows the connection to be made with a minimum amount of oxidation and without exposing the poly layers to an excessive amount of etching.

As discussed above, the Manley et al. patent does not teach a non-volatile memory structure having a floating gate extension structure that connects to the top of the floating gate, nor is there any teaching anywhere in the patent that motivate or suggest the forming of such structure. Consequently, it would not be obvious for someone with ordinary skill in the art to come up with the present invention after reading the Manley et al. patent. Therefore, Applicants assert that the amended claim 1 and the remaining dependent claims that depend on it have not been anticipated by the cited prior art and should be patentable.

Conclusion

Applicants assert that the amendment made to the claims does not incorporate any new matter. In view of the amendments and remarks made herein, Applicants request reconsideration of claims 1-8. A Notice of Allowance is earnestly solicited.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Asst. Commissioner for Patents, Washington, D.C. 20231

Signed: Sally Azevedo

Typed Name: Sally Azevedo

Date: July 31, 2002

Respectfully submitted,

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Version with Markings to Show Changes Made

1. (amended) A non-volatile memory cell comprising:

a semiconductor substrate, with a drain and a source in said substrate;

a floating gate formed on said substrate, said floating gate including a main floating gate region and a small sidewall spacer electrically coupled together by a connecting layer, said connecting layer being formed over and in contact with both said small sidewall spacer and said main floating gate region;

a first insulating layer separating said floating gate from said substrate, said first insulating layer including a first insulating portion and a second insulating portion, said first insulating portion separating said small sidewall spacer from said substrate, said second insulating portion separating said main floating gate region from said substrate, wherein, said first insulating portion is thinner than said second insulating portion;

a control gate formed over said floating gate; and

a second insulating layer separating said control gate and said floating gate.